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PATENT APPLICATION

Harold Alexis HUGGINS

CASE NO.: Huggins 6 (58638)

TITLE: METHOD FOR MAKING A RADIO FREQUENCY COMPONENT AND COMPONENT PRODUCED THEREBY

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

Enclosed are the following papers relating to the above-named application for patent::

Patent Application: 15 pages, 35 claims
2 Sheets of drawings
Assignment with Cover Sheet
Declaration and Power of Attorney
Information Disclosure Statement

The filing fee has been calculated as shown below:

CLAIMS AS FILED								
	(Col. 1)		(Col. 2)	SMALL ENTITY			LARGE ENTITY	
FOR:	# FILED		# EXTRA	RATE	FEE		RATE	FEE
BASIC FEE					$ 355	OR		$ 710
TOTAL CLAIMS	35	-20	15	X 9	$	OR	X 18	$ 270
INDEP CLAIMS	4	- 3	1	X 40	$	OR	X 80	$ 80
[ ] MULTIPLE DEPENDENT CLAIM PRESENTED				+	$	OR		
* If the difference in Col. 1 is less than "0", enter "0" in Col. 2.				TOTAL	$ ***		TOTAL	$ 1,060

Please file the application and charge **Lucent Technologies Deposit Account No. 12-2325** the amount of $1,060.00 to cover the filing fee. Duplicate copies of this letter are enclosed. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or credit **Deposit Account No. 12-2325** as required to correct the error.

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Telephone calls should be made to **CHRISTOPHER F. REGAN** at **(407) 841-2330**.

Respectfully,

November 17, 2000
Date

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METHOD FOR MAKING A RADIO FREQUENCY COMPONENT AND COMPONENT PRODUCED THEREBY

Field of the Invention

The present invention relates to the field of electronic circuits, and, more particularly, to methods for forming electronic circuits on dielectric layers.

Background of the Invention

Radio frequency (RF) devices and integrated circuits (ICs), such as inductors and capacitors, are well known for use in telecommunications applications. Many such devices and circuits are now being formed using thin dielectric layers or "membranes" made out of materials such as silicon nitride (SiN), for example. Such membranes have been found to improve the electrical characteristics of RF circuits mounted thereon. These membranes are typically formed on a substrate of suitable material, and the RF circuit is thereafter formed on the membrane which supports the RF circuit. The substrate provides support for the membrane during the patterning. Yet, capacitive coupling may occur between the substrate and the RF component, leading to device performance degradation.

To overcome this limitation, the RF component may be separated from the substrate. Prior art methods

for removing the RF component from the substrate typically require etching a window through an opposite side of the substrate to release the membrane. This so-called "backside" etching may include using hot potassium hydroxide (KOH) to etch a silicon substrate, for example, where the dielectric layer acts as an etch stop layer. One difficulty with backside etching is that it requires careful double-sided alignment to make sure that the etched area corresponds with the membrane. Furthermore, due to the corrosiveness of the KOH, any exposed portions of the substrate must be protected from the etchant, e.g., by using a mask. Having to deposit and remove such a mask requires additional processing time and costs. Also, the etch rate of KOH is about 100 μm per hour. As a result, typical etch times for an eight inch wafer, for example, may be seven hours or greater.

A prior art technique which addresses some of the difficulties associated with backside etching is disclosed in U.S. Patent No. 5,853,601 to Krishaswamy et al. entitled "Top-Via Etch Technique for Forming Dielectric Membranes." The patent is directed to methods for forming film bulk acoustic resonators (FBAR). The structure of an FBAR includes a substrate having a cavity on a surface thereof, a membrane on the substrate extending over the surface cavity, a first electrode on the membrane, a piezoelectric layer on the first membrane, and a second electrode layer on the piezoelectric layer. The method disclosed in the patent includes forming vias or openings through the membrane layer and isotropically etching the substrate through the vias using a dry etch process including an SF_6 gas. While this method does address the difficulty of backside alignment, it does not teach how to release the RF component from the substrate. Furthermore, the

etching process disclosed in the patent still requires a relatively long etch time due to the nature of the reactive ion etchant. Such an etchant may also damage delicate circuit components of RF circuits like those described above.

Summary of the Invention

In view of the foregoing background, it is therefore an object of the invention to provide a method for making a radio frequency (RF) component on a dielectric layer which alleviates the above noted problems associated with the prior art.

This and other objects, features, and advantages in accordance with the present invention are provided by a method for making an RF component including forming a dielectric layer on a semiconductor substrate and forming and patterning a conductive layer on the dielectric layer to define the RF component. The dielectric layer may include SiN, the conductive layer may include aluminum, and the semiconductor substrate may include silicon, for example. At least one opening may be formed through the RF component at least to the semiconductor substrate. Moreover, the at least one opening may either extend into the semiconductor substrate or substantially terminate at a surface of the semiconductor substrate. The RF component may then be released from the semiconductor substrate by exposing the semiconductor substrate to an etchant passing through the at least one opening to the semiconductor substrate.

Releasing the RF component may include exposing the semiconductor substrate to a dry etchant, such as XeF_2, for example. The at least one opening may have a diameter in a range of about .5 to 20 μm. Also, forming the at least one opening may include forming a

plurality of openings laterally adjacent to portions of the conductive layer with no openings extending through the conductive layer. The plurality of openings may be formed in a predetermined pattern having substantially uniform spacing between adjacent openings, where the substantially uniform spacing is in a range of about 20 to about 200 μm, for example.

An RF component according to the invention is also provided. The RF component may include a dielectric layer having opposing first and second major surfaces, the first surface being free from a semiconductor substrate, the dielectric layer having a plurality of openings extending between the first and second opposing major surfaces. The RF component may also include a patterned conductive layer on the second major surface of the dielectric layer.

Brief Description of the Drawings

FIG. 1 is a cross-sectional diagram of a semiconductor substrate having a dielectric layer formed thereon according to the present invention.

FIG. 2 is a cross-sectional diagram of the semiconductor substrate of FIG. 1 after the dielectric layer is patterned.

FIG. 3 is a cross-sectional diagram of the semiconductor substrate and patterned dielectric layer of FIG. 2 after the formation of a conductive layer thereon.

FIG. 4 is a cross-sectional diagram of the semiconductor substrate, patterned dielectric layer and conductive layer of FIG. 3 after patterning of the conductive layer to thereby form an RF component.

FIG. 5 is a top view showing the patterned conductive layer of FIG. 4.

FIG. 6 is a cross-sectional view of the semiconductor substrate and patterned dielectric and conductive layers of FIG. 4 after forming openings in the dielectric layer.

FIG. 7 is a top view showing the openings of FIG. 6.

FIG. 8 is a cross-sectional view of the semiconductor substrate and patterned dielectric and conductive layers for FIG. 6 illustrating releasing of the patterned and conductive dielectric layers from the semiconductor substrate.

FIG. 9 is a perspective view of an RF component according to the present invention.

Detailed Description of the Preferred Embodiments

The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout. Also, the dimensions of layers and regions may be exaggerated in the figures for greater clarity.

Referring now to the cross-sectional view of FIG. 1, a method for making a radio frequency (RF) component is first described. The method includes forming a dielectric layer **11** on a semiconductor substrate **12**. The semiconductor substrate **12** may include silicon and the dielectric layer **11** may include

SiN, for example. The dielectric layer **11** may be formed using conventional techniques known to those in the art (e.g., chemical vapor deposition). The dielectric layer **11** may then be patterned, again using conventional techniques, as shown in FIG. 2.

A conductive layer **13** is then formed using conventional techniques on the dielectric layer **11** (FIG. 3). The conductive layer **13** may the be patterned to define an RF component **10**, as shown in FIGS. 4 and 5. Again, conventional lithographic and etch techniques known in the art may be used to pattern the conductive layer **13**. The conductive layer may be aluminum, for example, although those of skill in the art will appreciate that other suitable conductors may be used as well. The conductive layer **13** of a typical RF component may be patterned to be an inductor or a capacitor, for example, though other circuit configurations are also possible.

At least one opening **14** is then formed through the RF component **10** at least to the semiconductor substrate **12**, as seen in FIG. 6. In the illustrated example, six openings are formed in the RF component **10**, as can be seen in the top view of FIG. 7. Of course, any number of openings **14** may be formed and the number selected will depend upon the size and shape of the component, the materials being used, etc., as will be appreciated by those of skill in the art. Specifically, the openings may substantially terminate at a surface of the semiconductor substrate **12**, as shown in FIG. 6, or extend into the semiconductor substrate (not shown). The openings **14** may be formed using conventional lithographic and etch techniques, for example, as will be appreciated by those of skill in the art.

The openings **14** are preferably formed laterally adjacent portions of the conductive layer **13** with no openings extending through the conductive layer. Furthermore, the openings **14** may be formed in a predetermined pattern with substantially uniform spacing between adjacent openings. For example, the substantially uniform spacing may be in a range of about 20 to about 200 μm. Also, each of the openings **14** may have a diameter in a range of .5 to 20 μm, for example.

The RF component **10** may then be released from the semiconductor substrate **12** by exposing the semiconductor substrate to an etchant passing through the openings **14** to the semiconductor substrate, as illustrated in FIG. 8. The etchant may be a dry etchant, such as xenon difluoride (XeF_2) gas, for example. The XeF_2 may be used to etch silicon isotropically at a rate in a range of up to about 10 μm per minute, for example. Furthermore, by appropriately spacing the predetermined pattern of openings **14** for a given RF component, the semiconductor substrate **12** only needs to be etched in small amounts in each of the defined regions. The combination of the increased etch rate of XeF_2 and appropriate selection of the predetermined pattern significantly reduces the time required to release the RF component **10** from the semiconductor substrate **12** compared to prior art methods, as will be appreciated by those of skill in the art. By way of example, a typical etch time to release an RF component from a silicon substrate according to the invention may be about 20 minutes or less.

Additionally, XeF_2 is much less corrosive than prior art etchants, such as KOH and the like. As a

result, the XeF_2 will have little effect on the RF component **10**, so a mask need not be used to protect the RF component. Avoiding such a masking step not only reduces the complexity of manufacturing an RF component but also results in savings in time and costs. Additionally, if silicon, for example, is included in the conductive layer **13**, the material (e.g., photoresist) used to define the pattern for the openings **14** would also serve to protect any exposed silicon from being etched, which would also further prevent additional process steps and reduce production time. The photoresist material will also protect exposed portions of the semiconductor substrate **12** from being unintentionally etched, as will be appreciated by those of skill in the art. Of course, those of skill in the art will also appreciate that the above described method also obviates the need for backside etching, which again reduces processing complexity and costs.

A completed RF component **10** made as described above may be seen in the perspective view of FIG. 9. The RF component **10** includes a dielectric layer **11** having opposing first and second major surfaces **15,16,** respectively. As can be seen, the first surface **15** is free from the semiconductor substrate **12.** The dielectric layer **11** has a plurality of openings **14** extending between the first and second opposing major surfaces **15, 16.** The RF component **10** also includes a patterned conductive layer **13** on the second major surface of said dielectric layer. The size, placement, and depth of the plurality of openings **14** may be similar to those described above. Each opening **14** may also have respective rounded over edges **17** adjacent the first and second major surfaces **15, 16** formed during

etching of the openings **14**, as will be appreciated by those of skill in the art.

Other devices and techniques using XeF_2 are disclosed in co-pending patent U.S. patent application, serial no. 09/637,069, filed August 11, 2000, also assigned to present assignee, which is hereby incorporated herein in its entirety by reference. In addition, many modifications and other embodiments of the invention will come to the mind of one skilled in the art having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is to be understood that the invention is not to be limited to the specific embodiments disclosed, and that other modifications and embodiments are intended to be included within the scope of the appended claims.

THAT WHICH IS CLAIMED IS:

1. A method for making a radio frequency (RF) component comprising:

forming a dielectric layer on a semiconductor substrate;

forming and patterning a conductive layer on the dielectric layer to define the RF component;

forming at least one opening through the RF component at least to the semiconductor substrate; and

releasing the RF component from the semiconductor substrate by exposing the semiconductor substrate to an etchant passing through the at least one opening to the semiconductor substrate.

2. The method of Claim 1 wherein releasing comprises exposing the semiconductor substrate to a dry etchant.

3. The method of Claim 2 wherein the dry etchant comprises XeF_2

4. The method of Claim 1 wherein forming the at least one opening comprises forming a plurality of openings laterally adjacent portions of the conductive layer with no openings extending through the conductive layer.

5. The method of Claim 1 wherein forming the plurality of openings comprises forming the plurality of openings in a predetermined pattern.

6. The method of Claim 5 wherein the predetermined pattern has substantially uniform spacing between adjacent openings.

7. The method of Claim 6 wherein the substantially uniform spacing is in a range of about 20 to about 200 μm.

8. The method of Claim 1 wherein the conductive layer comprises aluminum.

9. The method of Claim 1 wherein the dielectric layer comprises SiN.

10. The method of Claim 1 wherein forming the at least one opening comprises forming the at least one opening to have a diameter in a range of about .5 to 20 μm.

11. The method of Claim 1 wherein the semiconductor substrate comprises silicon.

12. The method of Claim 1 wherein the at least one opening extends into the semiconductor substrate.

13. The method of Claim 1 wherein the at least one opening substantially terminates at a surface of the semiconductor substrate.

14. A method for making a radio frequency (RF) component comprising:

forming a dielectric layer on a semiconductor substrate;

forming and patterning a conductive layer on the dielectric layer to define the RF component;

forming a plurality of openings through the dielectric layer at least to the semiconductor substrate; and

releasing the RF component from the semiconductor substrate by exposing the semiconductor substrate to an etchant passing through the openings to the semiconductor substrate.

15. The method of Claim 14 wherein releasing comprises exposing the semiconductor substrate to a dry etchant.

16. The method of Claim 15 wherein the dry etchant comprises XeF_2.

17. The method of Claim 14 wherein forming the plurality of openings comprises forming the plurality of openings in a predetermined pattern.

18. The method of Claim 17 wherein the predetermined pattern has substantially uniform spacing between adjacent openings.

19. The method of Claim 18 wherein the substantially uniform spacing is in a range of about 20 to about 200 μm.

20. The method of Claim 14 wherein the conductive layer comprises aluminum.

21. The method of Claim 14 wherein the dielectric layer comprises SiN.

22. The method of Claim 14 wherein the semiconductor substrate comprises silicon.

23. A method for making a radio frequency (RF) component comprising:

forming a dielectric layer on a semiconductor substrate;

forming and patterning a conductive layer on the dielectric layer to define the RF component;

forming a plurality of openings through the dielectric layer in a predetermined pattern at least to the semiconductor substrate; and

releasing the RF component from the semiconductor substrate by exposing the semiconductor substrate to an etchant comprising XeF_2 passing through the openings to the semiconductor substrate.

24. The method of Claim 23 wherein the predetermined pattern has substantially uniform spacing between adjacent openings.

25. The method of Claim 24 wherein the substantially uniform spacing is in a range of about 20 to about 200 μm.

26. The method of Claim 23 wherein the conductive layer comprises aluminum.

27. The method of Claim 23 wherein the dielectric layer comprises SiN.

28. The method of Claim 23 wherein the semiconductor substrate comprises silicon.

29. A radio frequency (RF) component comprising:

a dielectric layer having opposing first and second major surfaces, the first surface being free from a semiconductor substrate, said dielectric layer

having a plurality of openings extending between the first and second opposing major surfaces; and

a patterned conductive layer on the second major surface of said dielectric layer.

30. The RF component of Claim 29 wherein said plurality of openings are arranged in a predetermined pattern.

31. The RF component of Claim 30 wherein the predetermined pattern has substantially uniform spacing between adjacent openings.

32. The RF component of Claim 31 wherein the substantially uniform spacing is in a range of about 20 to about 200 μm.

33. The RF component of Claim 29 wherein each opening has a diameter in a range of about .5 to 20 μm.

34. The RF component of Claim 29 wherein each opening has respective rounded over edges adjacent the first and second major surfaces.

35. The RF component of Claim 29 wherein the plurality of openings are laterally adjacent portions of the conductive layer with no openings extending through the conductive layer.

METHOD FOR MAKING A RADIO FREQUENCY COMPONENT AND COMPONENT PRODUCED THEREBY

Abstract of the Disclosure

A method for making a radio frequency (RF) component includes forming a dielectric layer on a semiconductor substrate and forming and patterning a conductive layer on the dielectric layer to define the RF component. The dielectric layer may include SiN, the conductive layer may include aluminum, and the semiconductor substrate may include silicon, for example. At least one opening may be formed through the RF component at least to the semiconductor substrate. Moreover, the at least one opening may either extend into the semiconductor substrate or substantially terminate at a surface of the semiconductor substrate. The RF component may then be released from the semiconductor substrate by exposing the semiconductor substrate to an etchant passing through the at least one opening to the semiconductor substrate. Releasing the RF component may include exposing the semiconductor substrate to a dry etchant, such as XeF_2, for example.

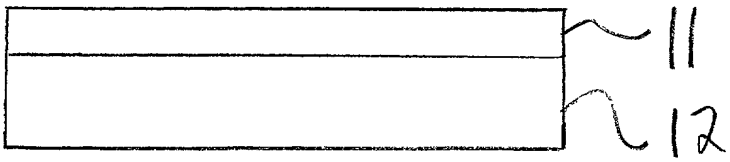

FIG. 1

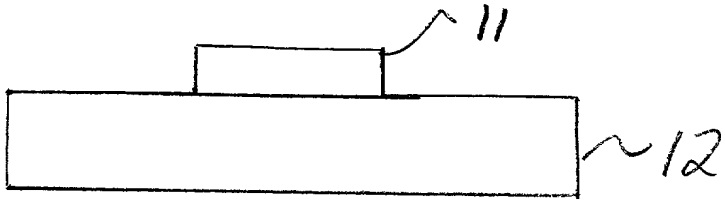

FIG. 2

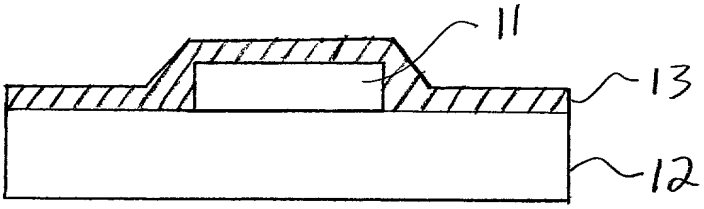

FIG. 3

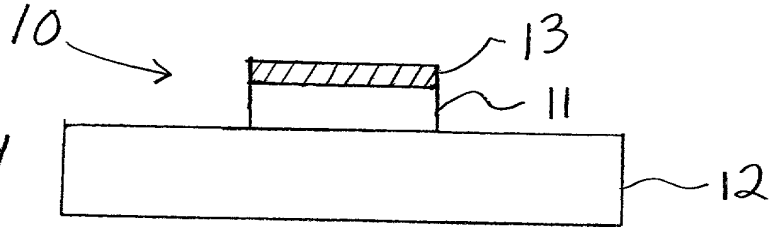

FIG. 4

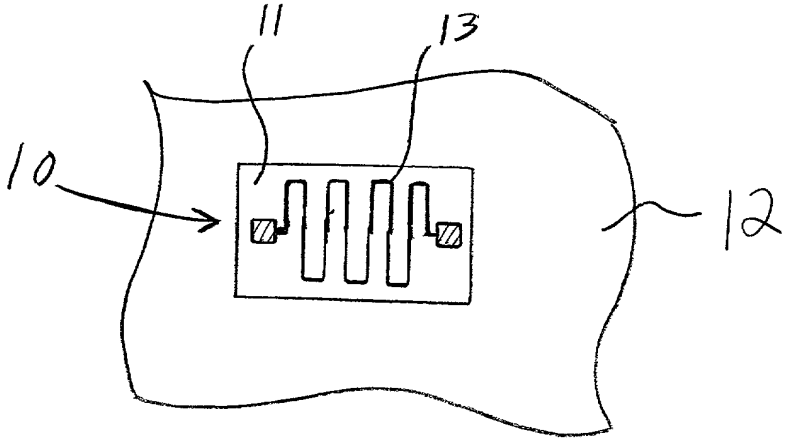

FIG. 5

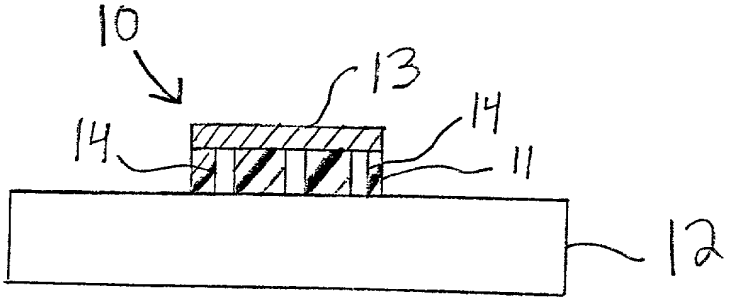

FIG. 6

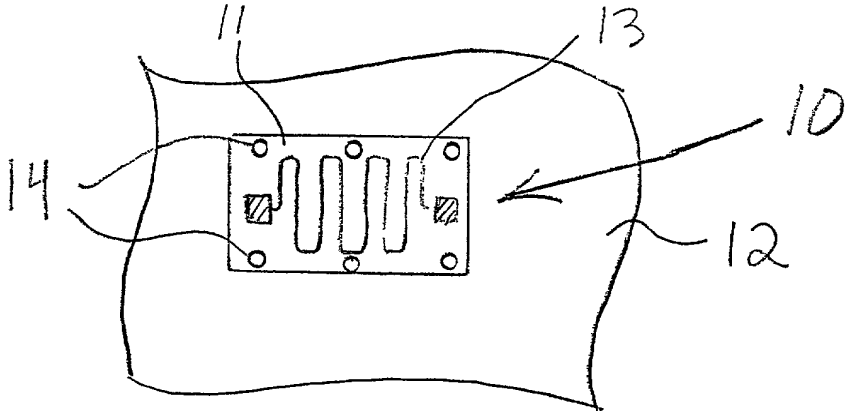

FIG. 7

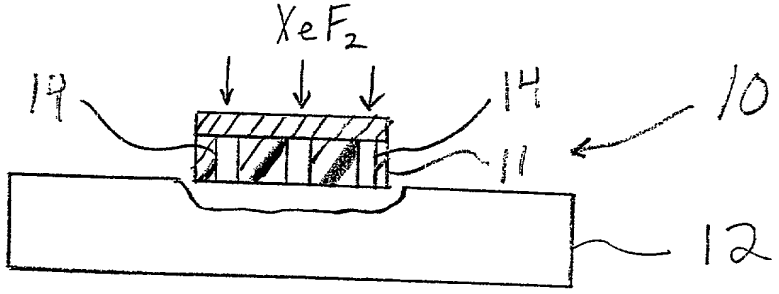

FIG. 8

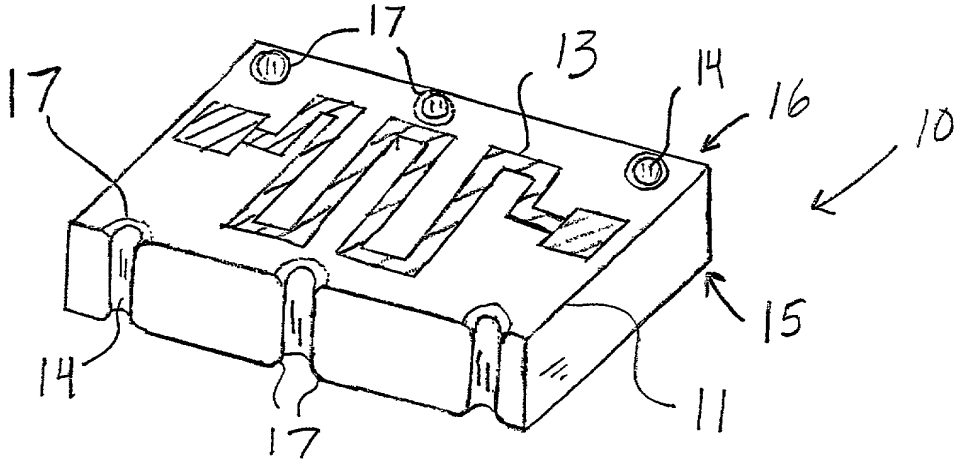

FIG. 9

Case Name and No. Huggins 6

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Declaration and Power of Attorney

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **METHOD FOR MAKING A RADIO FREQUENCY COMPONENT AND COMPONENT PRODUCED THEREBY** the specification of which ***is attached hereto.***

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) with full power of substitution and revocation, to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected therewith:

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Jeffery J. Brosemer	(Reg. No. 36096)
Kenneth M. Brown	(Reg. No. 37590)
Donald P. Dinella	(Reg. No. 39961)
Guy Eriksen	(Reg. No. 41736)
Martin I. Finston	(Reg. No. 31613)
William S. Francos	(Reg. No. 38456)
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Jack R. Penrod	(Reg. No. 31864)
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Ferdinand M. Romano	(Reg. No. 32752)
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I hereby appoint the attorney(s) on ATTACHMENT A as associate attorney(s) in the aforementioned application, with full power solely to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected with the prosecution of said application. No other powers are granted to such associate attorney(s) and such associate attorney(s) are specifically denied any power of substitution or revocation.

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Inventor's signature Harold Alexis Huggins Date 11/16/00

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	Charles E. Wands	25,649
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